NORCAS 2016

Technical Programme

Tuesday 1 November

1. Opening

Chair: Jari Nurmi, Tampere University of Technology, FI

09.00 **Opening and welcome**
Jari Nurmi, Tampere University of Technology, FI
Jens Sparsø, Technical University of Denmark, DK

09.15 **Invited talk: Auto-adaptive digital circuits – Application to low-power Multicores and ultra-low-power Wireless Sensor Nodes**
Edith Beigne, CEA, FR

10.00 A 1.3-uW 12-bit Incremental Delta-Sigma ADC for Energy Harvesting Sensor Applications
Shiva Jamali-Zavareh[1], Jarno Salomaa[2], Mika Pulkkinen[2], Shailesh singh Chouhan[2], Kari Halonen[2], 1) University of Minnesota, USA and 2) Aalto University, FI

10.20 True Random Number Generation from Bang-Bang ADPLL Jitter
Felix Neumärker, Sebastian Höppner, Andreas Dixius, Christian Mayr, Technische Universität Dresden, DE

10.40 **Coffee break**

2.1 Multi-Core and NoC

Chair: Jari Nurmi, Tampere University of Technology, FI

11.10 High-Level NoC Model for MPSoC Compilers
Christian Menard, Andrés Goens, Jeronimo Castrillon, TU Dresden, DE

11.30 The REPLICA on-chip network
Martti Forsell[1], Jussi Roivainen[1], Ville Leppänen[2], 1) VTT, FI, 2) University of Turku, FI

11.50 Sensor Data Fusion with MPSoCSim in the Context of Electric Vehicle Charging Stations

2.2 RF and HF Circuits

Chair: Henrik Sjöland, Lund University, SE

A Wideband Blocker-Resilient RF Front-End With Selective Input-Impedance Matching for Direct-Delta-Sigma-Receiver Architectures
Faizan Ul haq[1], Mikko Englund1, Kari Stadius[1], Marko Kosunen[1], Jussi Ryynänen1, Kimmo Koli[2], Kim B Östman[3], 1) Aalto University, FI, 2) Huawei Technologies Oy Co. Ltd, FI, 3) Nordic Semiconductor, FI

A 4.5 mW, 0.01148 mm2 frequency multiplier based on DLL with output frequency from 4 to 6 GHz
Erkan Bayram, Oner Hanay, Renato Negra RWTH Aachen University, DE

Multiphase Digitally Controlled Oscillator for Future 5G Phased Arrays in 90 nm CMOS

Ivan Stoychev, Philipp Wehner, Jens Rettkowski, Tobias Kalb, Diana Göhringer, Jürgen Oehm, Ruhr University, DE

Arnout Devos, Marco Vigilante, Patrick Reynaert
KU Leuven, BE

12.10 Accelerating MPSoC Design Space Exploration Within System-Level Frameworks
Syed Abbas Ali Shah, Bastian Farkas, Rolf Meyer, Mladen Berekovic, TU Braunschweig, DE

20-300 MHz Frequency Generator with -70 dBc Reference Spur for Low Jitter Serial Applications
Gurkan Yilmaz, Catherine Dehollain, Ecole Polytechnique Federale de Lausanne, CH

12.30 **Lunch**

3.1 Memory

Chair: Joachim Rodrigues, Lund University, SE

3.2 Low Power/Low Voltage

Chair: Markku Åberg, VTT, FI

13.40 Design and Simulation of a Quaternary Memory Cell based on a Physical Memristor
Jonathan Taylor, Alberto Nannarelli, Technical University of Denmark, DK

A CMOS MF Energy Harvesting and Data Demodulator Receiver for Wide Area Low Duty Cycle Applications with 230 mV Start-Up Voltage
Teerasak Lee[1], Henry Kennedy[1], Rares Bodnar[1,2], William Redman-White[1], 1) University of Southampton, UK, 2) Analog Devices, UK

14.00 An OR-Type Cascaded Match Line Scheme for HighPerformance and EDP-Efficient Ternary Content Addressable Memory
Jianwei Zhang, Shanxing Zheng, Fei Teng, Qiuhong Ding, Xiaoming Chen, Dalian University of Technology, CN

Capacitor-Free, Low Drop-Out Linear Regulator in a 180 nm CMOS for Hearing Aids
Yoni Yosef-Hay, Pere Llimos Muntal, Dennis Øland Larsen, Ivan H.H. Jørgensen, Technical University of Denmark, DK

14.20 DRAM Row-Hammer Attack Reduction Using Dummy Cells
Hector Gomez, Andres Amaya, Elkim Roa, Universidad Industrial de Santander, CO

Fully Integrated Triple-Mode Sigma-Delta Modulator for Speech Codec
Lei Zou[1], Marco De Blasi[1], Gino Rocca[1], Marco Grassi[2], Piero Malcovati[2], Andrea Baschirotto[3], 1) EPCOS AG, DK 2) University of Pavia, IT, 3) University of Milano-Bicocca, IT

4. Poster session I

14.40 **Analog circuits**

Oscillation Ring Testing Methodology of TSVs in 3D Stacked ICs
Shadi Harb, Intel Corporation, USA

Optimizing simulation times in biomedical systems containing Quasi-Infinite Resistors
Saam Iranmanesh, Majd Eid, Esther Rodriguez-villegas, Imperial College London, UK

Performance evaluation of classical differential rectifier by using forward body biasing technique
Shailesh Singh Chouhan, Kari Halonen, Aalto University, FI

Design of a VCO-based ADC in 28 nm FDSOI CMOS
Vishnu Unnikrishnan, Mark Vesterbacka, Linköping University, SE

Digital

A novel random approach to diagnostic test generation
Emmanuel Ovie Osimiry, Raimund Ubar, Sergei Kostin, Jaan Raik, Tallinn University of Technology, EE

Data Type Dependent Energy Consumption Estimation

Priit Ruberg, Keijo Lass, Peeter Ellervee, Tallinn University of Technology, EE

Area and Power Consumption Trade-off for Sigma - Delta Decimation Filter in Mixed Signal Wearable IC
Alessandro Palla, Gabriele Meoni, Luca Fanucci, University of Pisa, IT

Natural logarithm and division floating-point high throughput co-processor implemented in FPGA
Peter Malik, Slovak Academy of Sciences, SK

15.30 **Invited talk: Near-threshold and sub-threshold memories**
Joachim Rodrigues, Lund University, SE

5.1 IoT and Energy Sources

Chair: Peeter Ellervee, Tallinn University of Technology, EE

16.15 IoT-Based Fall Detection System with Energy Efficient Sensor Nodes
Tuan Nguyen Gia1, Igor Tcarenko1, Victor K. Sarker[1], Amir M. Rahmani[1], Tomi Westerlund[1], Pasi Liljeberg[1], Hannu Tenhunen[1,2], 1) University of Turku, FI, 2) KTH Royal Institute of Technology, SE

16.35 Solar panel modelling for low illuminance indoor conditions
Xinyu Ma, Sebastian Bader, Bengt Oelmann, Mid Sweden University, SE

16.55 Simulation of New Impulsional Current Profile For Lithium-ion Battery Test
Zine Elabadine Dahmane[1], Mohamed Salah Ait Cheikh[2], Mustapha Bouhali[1], Moussaab Bounabi1, Karim Kaced[1], 1) Ecole Nationale Polytechique Alger, DZ, 2) Ecole Polytechnique Oran, DZ

5.2 Application-Specific Hardware

Chair: Waqar Hussain, Tampere University of Technology, FI

16.15 CPCIe: A Compression-enabled PCIe Core for Energy and Performance Optimization
Mohd Amiruddin Zainol, Jose Luis Nunez-Yanez, University of Bristol, UK

16.35 Dynamically Reconfigurable Real-Time Hardware Architecture for Channel Utilisation Analysis in Industrial Wireless Communication
Ludwig Sebastian Karsthof[1], Mingjie Hao[1], Jochen Rust[1], Steffen Paul[1], Uwe Meier[2], Dimitri Block[2], 1) University of Bremen, DE, 2) Ostwestfalen-Lippe University of Applied Sciences, DE

16.55 FPGA Implementation and Integration of a Reconfigurable CAN-Based Coprocessor to the COFFEE RISC Processor
Farid Shamani, Vida Fakour Sevom, Tapani Ahonen, Jari Nurmi, Tampere University of Technology, FI

17.15 Break

19.00 **Dinner**

Wednesday 2 November

09.00 **Invited talk: The Existence of Dark Silicon in the Internet-of-Everything Universe - Can we find another World?**
Waqar Hussain, Tampere University of Technology, FI

6. Poster session II

Coffe break

09.45 **SoC**

Exclusive Control for Compound Operations on Hardware Transactional Memory

Keisuke Mashita, Anju Hirota, Tomoaki Tsumura, Nagoya Institute of Technology, JP

Distributed SystemC Simulation on Manycore Servers
Janne Virtanen, Panu Sjövall, Marko Viitanen, Timo D. Hämäläinen, Jarno Vanne, Tampere University of Technology, FI

A Special Processor Design for Nucleotide Basic Local Alignment Search Tool with a New Banded Two-Hit Method
Chih-Yu Chang, Yu-Cheng Li, Nae-Chyun Chen, Xiao-Xuan Huang, Yi-Chang Lu, National Taiwan University, TW

Automatic Generation of RTL Connectivity Checkers for Automotive Gateways from SystemC TLM Models
Tomas Grimm[1], Djones Lettnin[2], Michael Hübner[1], 1) Ruhr-Universität Bochum, DE, 2) Federal University of Santa Catarina, BR

Analog circuits

Area-Efficiency Trade-Offs in Integrated Switched-Capacitor DC-DC Converters
Frederik Monrad Spliid, Dennis Øland Larsen, Arnold Knott, Technical University of Denmark, DK

An experimental comparison between two widely adopted phase noise models
Federico Pepe, Pietro Andreani, Lund University, SE

Voltage multiplier arrangement for heavy load conditions in RF energy harvesting
Shailesh Singh Chouhan, Kari Halonen, Aalto University, FI

6.1 Arithmetic and Clocking

Chair: Atila Alvandpour, Linköping University, SE

10.30 Ultra-Low Voltage Adders in 28 nm FDSOI Exploring Poly-Biasing for Device Sizing
Ali Asghar Vatanjou, Even Låte, Trond Ytterdal, Snorre Aunet, NTNU, NO

10.50 Bivariate Function Approximation with Encoded Gradients
Jochen Rust, Steffen Paul, University of Bremen, DE

11.10 Hierarchical Design of a Low Power Standing Wave Oscillator Based Clock Distribution Network
Zhang Wei, Hu Youde, Cui Keji, Bao Dongxuan, Pan Dashan, Wang Lebo, Zheng Lirong, Fudan University, CN

11.30 A Fully-Synthesized TRNG with Lightweight Cellular-Automata Based Post-Processing Stage in 130nm CMOS
Juan Cartagena, Hector Gomez, Elkim Roa, Universidad Industrial de Santander, CO

11.50 **Lunch**

6.2 Data Converters

Chair: Kari Halonen, Aalto University, FI

13-Bit RF-DAC up to 14 GS/s at 3.5 GHz introducing Smart-Switching
Lukas Fraeger, Oner Hanay, Erkan Bayram, Renato Negra, RWTH Aachen University, DE

Current-Steering DAC Linearisation by Impedance Transformation
Stefan Mueller, Oner Hanay, Renato Negra, RWTH Aachen University, DE

A Current-Mode Analog-to-Time Converter with Short-Pulse Output Capability Using Local Intra-Cell Activation for High-Speed Time-Domain Biosensor Array
Kei Ikeda1, Atsuki Kobayashi[1], Kazuo Nakazato[1], Kiichi Niitsu[1,2], 1) Nagoya University, JP, 2) PRESTO, JST, JP

A 10MHz Bandwidth Continuous-Time Delta-Sigma Modulator for Portable Ultrasound Scanners
Pere Llimós Muntal, Ivan H.H. Jørgensen, Erik Bruun, Technical University of Denmark, DK

7. Plenary Session

Ivan Jørgensen, Technical University of Denmark, DK

13.00 **Invited talk: How to combine low cost, high efficiency, small size and flexibility? - CMOS integrated power management to the rescue!**
Filip Tavernier, KU Leuven, Belgium

13.45 A 2 GHz Low Noise Amplifier with Transformer Input Matching in 28 nm CMOS
Robert Kostack[1,2], Christoph Tzschoppe[2], Herbert Stockinger[1], Udo Jörges[2], Frank Ellinger[2], 1) Intel Deutschland GmbH, DE; 2) Technische Universität Dresden, DE

14.05 A Database Accelerator for Energy-Efficient Query Processing and Optimization
Sebastian Haas[1], Oliver Arnold[1], Stefan Scholze[1], Sebastian Höppner[1], Georg Ellguth[1], Andreas Dixius[1], Annett Ungethüm[1], Eric Mier[1], Benedikt Nöthen[1], Emil Matus[1], Stefan Schiefer[1], Love Cederstroem[1], Fabian Pilz[2], Christian Mayr[1], René Schüffny[1], Wolfgang Lehner[1], Gerhard Fettweis[1], 1) TU Dresden, DE, 2) RacyICs GmbH, DE

14.25 NorCAS 2017 announcement

14.30 Coffee

8.1 OpenCL Computing

Chair: Jens Sparsø, Technical University of Denmark, DK

15.00 Energy Proportional Computing with OpenCL on a FPGA-Based Overlay Architecture
Awais Hussain Sani, Jose Luis Nunez Yanez, Bristol University, UK

15.20 OpenCL Programmable Exposed Datapath High Performance Low-Power Image Signal Processor
Joonas Iisakki Multanen[1], Heikki Kultala[1], Matias Koskela[1], Timo Viitanen[1], Pekka Jääskeläinen[1], Jarmo Takala[1], Aram Danielyan[2], Cristóvão Cruz[2], 1) Tampere University of Technology, FI, 2) Noiseless Imaging Ltd, FI

15.40 Using OpenCL to Rapidly Prototype FPGA Designs
Kui Wang, Jari Nurmi, Tampere University of Technology, FI

8.2 Analog and Mixed-Mode Systems

Chair: Markku Åberg, VTT, FI

A CMOS 16k Microelectrode Array as Docking Platform for Autonomous Microsystems
Lukas Straczek, Dominic Alexander Funke, Abhishek Sharma, Thomas Maeke, John S. McCaskill, Jürgen Oehm, Ruhr-University Bochum, DE

Current Driver with Read-Out HV Protection for Neural Stimulation
Dmitry Osipov, Steffen Paul, Serge Strokov, Andreas K. Kreiter, Andreas Schander, Tobias Tessmann, Walter Lang,University of Bremen, DE

Asynchronous Clock Generator for a 14-bit Two-stage Pipelined SAR ADC in 0.18 µm CMOS
Kairang Chen, Martin Nielsen-Lönn, Atila Alvandpour, Linköping University, SE

16.00 Finish

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