NORCAS 2015

Technical Programme

Monday 26 October

Tutorial: Frequency Generation for the Internet of Things
Lecturer: Danielle Griffith, TI, USA

13.00 Introduction to oscillators used in IoT radios
Low power requirements vs the oscillator architecture
Sleep power and the sleep timer frequency stability
Description of oscillators that can be used as a sleep timer
Design examples and power/accuracy tradeoffs
Description of possible architectures, design examples, and tradeoffs

17.00 Finish

Tuesday 27 October

1. Opening

Chair: Jim Tørresen, University of Oslo, NO

09.00 **Opening and welcome**
Tor S. Lande, University of Oslo, NO
Jim Tørresen, University of Oslo, NO

09.15 **Invited talk: The All Programmable SOC FPGA at the heart of embedded systems**
Ivo Bolsens, Xilinx, US

10.00 Long-Term ECG Monitoring with Zeroing Compressed Sensing Approach
Mangia, Mauro; Bortolotti, Daniele; Bartolini, Andrea; Pareschi, Fabio; Benini, Luca; Rovatti, Riccardo; Setti, Gianluca, University of Bologna, IT

10.20 Digital Background Calibration in Continuous-time Delta-Sigma Analog to Digital Converters
Tan, Siyu; Miao, Yun; Palm, Mattias; Rodrigues, Joachim; Andreani, Pietro, Lund University, SE

10.40 **Coffee break**

2.1 Data Converters

Chair: Peter Nilsson, Lund University, SE

11.10 A 10-bit Reference Free Current Mode SAR ADC with 58.4 dB SFDR at 50 MS/s in 90 nm CMOS

2.2 Reconfigurable Architectures

Chair:Waqar Hussain, Tampere University of Technology, FI

Executing Secured Virtual Machines within a Manycore Architecture
Dévigne, Clément; Bréjon, Jean-Baptiste;

Elkafrawy, Abdelrahman; Anders, Jens; Ortmanns, Maurits, University of Ulm, DE

Meunier, Quentin; Wajsbürt, Franck, Université Pierre et Marie Curie, FR

11.30 An Ultra Low Power Biomedical Signal Acquisition System Powered by A -22 dBm RF Energy Harvesting Circuit
Patra, Pravanjan; Yadav, Kunal; Naik, Jairaj; Dutta, Asudeb, Indian Institute of Technology Hyderabad, IN

Design, Implementation and Analysis of a Run-time Configurable Memory Management Unit on FPGA
Shamani, Farid; Fakour Sevom, Vida; Nurmi, Jari; Ahonen, Tapani, Tampere University of Technology, FI

11.50 Fundamental Power Limits of SAR and ΔΣAnalog-toDigital Converters
Brenna, Stefano; Bettini, Luca; Bonfanti, Andrea; Lacaita, Andrea Leonardo, Andrea Bonetti,
Politecnico di Milano, IT

Empirical Results on Parity-based Soft Error Detection with Software-based Retry
Aydos, Gökçe; Fey, Görschwin, University of Bremen, DE

12.10 A Fully Synthesized All-Digital VCO-Based Analog-to-Digital Converter
Vishnu Unnikrishnan, Srinivasa Rao Pathapati and Mark Vesterbacka, Linköping University, SE

Fault Tolerant Field Programmable Neural Networks
Krčma, Martin; Kotásek, Zdeněk; Kaštil, Jan, Faculty of Information Technology, Brno University of Technology, CZ

12.30 System Level Design of a Continuous-Time Sigma-Delta Modulator for Portable Ultrasound Scanners
Llimos Muntal, Pere; Færch, Kjartan; Jørgensen, Ivan H.H.; Bruun, Erik, Technical University of Denmark, DK

Secured-by-Design FPGA: Look-Up Tables and Switch-Boxes
Almohaimeed, Ziyad; Sima, Mihai, University of Victoria, CA

12.50 **Lunch**

3.1 PLLs

Chair: Jorma Skyttä, Aalto University, FI

3.2 Communication Technology

Chair: Peeter Ellervee, Tallinn University of Technology, EE

14.00 A BW-tracking semi-digital PLL with near-optimal VCO phase noise shaping in low-cost 0.4 µm CMOS achieving 700 fs rms phase jitter
Fahmy, Said; Sareen, Puneet; Dietl, Markus; Ortmanns, Maurits; Anders, Jens, University of Ulm, DE

Carrier Frequency and Sampling Rate Offsets Effect on Sub 6 GHz Massive MIMO
Ahmed-Ouameur, Messaoud; Massicotte, Daniel; Zhu, Wui-Ping, Universite du Quebec a Trois-Rivieres, CA

14.20 A 65nm CMOS Fraction-N Digital PLL with Shaped Inband Phase noise
Mahmoud, Ahmed; Andreani, Pietro; Lu, Ping, Lund University, SE

Parallel Independent FFTs Implementation on Intel Processors and Xeon Phi for LTE and OFDM Systems
Khelifi, Mounir; Massicotte, Daniel; Savaria, Yvon, Université du Québec à Trois-Rivières, CA

14.40 Tracking PVT variations of Pulse Width Controlled PLL using Variable-Length Ring Oscillator
Toi, Takashi; Nakura, Toru; Iizuka, Tetsuya; Asada, Kunihiro, The University of Tokyo, JP

Two-Variable Numeric Function Approximation Using Least-Squares-Based Regression,
Rust, Jochen; Heidmann, Nils; Paul, Steffen, University of Bremen, DE

4. Poster session I

15.00 **Analog circuits**

Ultra low-power, -area and -frequency CMOS thyristor based oscillator for autonomous microsystems
Funke, Dominic Alexander; Oehm, Jürgen; Mayr, Pierre; Maeke, Thomas; McCaskill, John Simpson; Sharma, Abhishek; Straczek, Lukas, Ruhr Universität Bochum, DE

Analysis and Design of a 1.1dB-IL third-order Matching Network for Switched-Capacitor PAs
Passamani, Antonio; Ponton, Davide; Knoblinger, Gerhard; Bevilacqua, Andrea, University of Padova, IT

A New Current Stimulator Architecture for Visual Cortex Stimulation
Osipov, Dmitry; Paul, Steffen; Strokov, Serge; Kreiter, Andreas K., University of Bremen, DE

A CMOS High Resolution Multi-Edge Delay Generator
Harb, Shadi; Eisenstadt, William, Intel Corporation, US

A Capacitor-Free, Fast Transient Response Linear Voltage Regulator In a 180nm CMOS
Deleuran, Alexander Nymann; Lindbjerg, Nicklas; Pedersen, Martin Kofoed; Llimós Muntal, Pere; Jørgensen, Ivan Harald Holger, Technical University of Denmark, DK

Single Chip Wireless Condition Monitoring of Power Semiconductor Modules
Nilsson, Joakim; Borg, Johan; Johansson, Jonny, Luleå University of Technology, SE

Performance Optimization of Conventional Schottky Barrier CNTFETs Based on Stair-Case Doped Strategy
Ghasemi Nejad Raeini, Amin; Kordrostami, Zoheir; faghei, Morteza; Sadeghi, Hamid, Gol e Gohar Mining and industrial co, Sirjan, IR

Ultra Low Power On-Chip Hybrid Start-Up for Wireless Sensor Networks
Vamsi, Nagaveni; Gupta, Akash; Dutta, Ashudeb; Singh, Shiv Govind, Indian Institute of Technology Hyderabad, IN

Full Swing 20 GHz Frequency Divider with 1 V Supply Voltage in FD-SOI 28 nm Technology
Ozsema, Hasene Gulperi; Kostak, Duygu; Demirci, Tugba; Leblebici, Yusuf, Swiss Federal Institute of Technology Lausanne (EPFL), CH

3.6 GHz CMOS Ring Oscillator with Low Tune Voltage Sensitivity and Temperature Compensation
Ozsema, Hasene Gulperi; Demirci, Tugba; Leblebici, Yusuf, Swiss Federal Institute of Technology Lausanne (EPFL), CH

System-on-Chip

A Hardware Architecture for the Branch and Bound Flow-Shop Scheduling Algorithm
Daouri, Mikhael; Escobar Juzga, Fernando Adolfo; Chang, Xin; Valderrama, Carlos, UMONS, BE

Interfacing Hardware Accelerators to a Time-Division Multiplexing Network-on-Chip
Pezzarossa, Luca; Sørensen, Rasmus Bo; Shoeberl, Martin; Sparsø, Jens, Technical University of Denmark, DK

Design of a Hybrid Multicore Platform for High Performance Reconfigurable Computing
Hussain, Waqar; Hoffmann, Henry; Ahonen, Tapani; Nurmi, Jari, Tampere University of Technology, FI

How Small and Still Effective a CMOS-SoC Could ever be?
Heusala, Hannu H.; Skytta, Jorma, Aalto University, FI

5.1 DC/DC converters

Chair: Johan Wernehag, Lund University, SE

15.50 High-Efficiency Peak-Current-Control Non-inverting Buck-Boost Converter Using Mode Selection for Single Ni-MH Cell Battery Operation
Kim, Jong-Seok; Lee, Jae-Yoon; Choi, Byong-Deok, Hanyang University, KR

16.10 Application of spread-spectrum techniques to class-E DC/DC converters: some preliminary results
Pareschi, Fabio; Vincenzi, Tommaso; Mangia, Mauro; Bertoni, Nicola; Rovatti, Riccardo; Setti, Gianluca, University of Ferrara, IT

5.2 Digital System Design

Chair: Jari Nurmi, Tampere University of Technology, FI

Fault-Tolerant Implementation of Direct FIR Filters Protected Using Residue Codes
Piestrak, Stanislaw; Patronik, Piotr, Wroclaw Univ. of Technology, PL

Low Power Unrolled CORDIC Architectures
Nilsson, Peter (1); Gangarajaiah, Rakesh (1); Sun, Yuhang (1); Hertz, Erik (2), 1 Lund University, 2 Halmstad University

16.30 **Invited talk: The electronics industry is suffering from bad priorities in the university education**

Espen Tallaksen, Bitvis, Norway

17.15 Break

19.00 **Dinner** (Thon Hotel Vika Atrium)

Wednesday 28 October

09.00 **Invited talk: Design Challenges for the Internet of Things**
Danielle Griffith, TI, US

6. Poster session II

Coffe break

09.45 **Digital systems**

A Novel Multiplexer-based 64-bit SRAM Design Using QCA
Karuppiah, Pandiammal; Deivasigamani, Meganathan, Jerusalem Collge of Engineering Chennai India, IN

Formal Analysis of Macro Synchronous Micro Asychronous Pipeline for Hardware Trojan Detection
Lodhi, Faiq Khalid; Hasan, Syed Rafay; Hasan, Osman; Awwad, Falah, National University of Sciences and Technology, PK

An Ultra-Low-Power/High-Speed 9-bit Adder Design: Analysis and Comparison Vs. Technology from 130nm-LP to UTBBFD-SOI-28nm
Atarzadeh, Hourieh; Aunet, Snorre; Yttedral, Trond, Norwegian University of Science and Technology, NO

The Low Delay Low-Pass FIR Digital Differentiators Having Flat Passband and Equiripple Stopband
Yoshida, Takashi; Aikawa, Naoyuki, Tokyo University of Science, JP

Architectural Design Space Exploration of an FPGA-based Compressed Sampling Engine: Application to Wireless Heart-Rate Monitoring
El-Sayed, Mohammad; Koch, Peter; Le Moullec, Yannick, Tallinn University of Technology, EE

A design platform for flexible programmable DSP for automotive sensor conditioning
Sisto, Arcangelo; Pilato, Luca; Serventi, Riccardo; Fanucci, Luca, University of Pisa, IT

Analog circuits

Wide band edge-coupled impedance matching network with quarter wavelength measurement circuit
Yadegar Amin, Hamid; Yarman, binboğa Sıddık, Istanbul Technical University, TU

Self-Biasing High-Voltage Driver Based on Standard CMOS with an Adapted Level Shifter for a Wide Range of Supply Voltages
Pashmineh, Sara; Killat, Dirk, Brandenburg University of Technology, DE

An Ultra Wide-Band Adaptive Frequency Divider For mm-wave PLL Applications
Athanasiadis, Pavlos; Mountrichas, Lampros; Siskos, Stylianos, Aristotle University of Thessaloniki, GR

A Low/High Band Highly Linearized Reconfigurable Down Conversion Mixer in 65nm CMOS Process
Gupta, Nisha; Dutta, Ashudeb; Singh, Shiv Govind, IIT Hyderabad, IN

Fixed pattern noise correction for wide dynamic range CMOS image sensor with Reinhard tone mapping Operator
Mughal, Waqas; Choubey, Bhaskar, University of Glasgow, UK

Evaluation of the Vertical Magnetic Field Generated by a Spiral Planar Coil
Minnaert, Ben; Stevens, Nobby, KU Leuven, BE

Frequency planning for a high SFDR digital-IF RF-DAC based transmitter
Hanay, Oner; Bayram, Erkan; Elsayed, Mohamed Saeed; Negra, Renato, RWTH Aachen University, DE

Design of a Highly Linear, Low Noise, Broad Band UpConverter for Cognitive Radio Applications

Varga, Gabor; Ashok, Arun; Subbiah, Iyappan; Schrey, Moritz; Heinen, Stefan, RWTH Aachen University, DE

A Noise Coupled ΣΔArchitecture using a Non Uniform Quantizer
Torreño Carrera, Juan Antonio; Patón Álvarez, Susana; Conesa-Peraleja, Laura; Straeussnigg, Dietmar; Hernández, Luis, Carlos III University Madrid, ES

6.1 "Mixed Analog"

Chair: Tor S. Lande, University of Oslo, NO

6.2 Modeling and simulation of embedded systems

Chair: Jari Nurmi, Tampere University of Technology, FI

10.30 A NAND Gate Based Standard Cell VCO for Use in Synthesizable ADCs
Unnikrishnan, Vishnu; Vesterbacka, Mark, Linköping University, SE

Design and Evaluation of Correlation Accelerator in IEEE-802.11a/g Receiver using a Template-based Coarse-Grained Reconfigurable Array
Nouri, Sajjad; Hussain, Waqar; Nurmi, Jari, Tampere University of Technology, FI

10.50 Process Tolerant Highly Linear Mixer Output Stage with Feedforward Linearity Improvement Method for a HighIF Converter
Ashok, Arun; Varga, Gabor; Subbiah, Iyappan; Schrey, Moritz; Heinen, Stefan, RWTH Aachen, DE

Test-Driven Modeling of Embedded Systems
Munck, Allan; Madsen, Jan, Technical University of Denmark, DK

11.10 On-Chip Spatial Filter for Subretinal Implants
Rieger, Viola; Schütz, Henning; Gambach, Stefan; Rothermel, Albrecht, University of Ulm, DE

Shared Structurally Synthesized BDDs for Speeding-Up Parallel Pattern Simulation in Digital Circuits
Ubar, Raimund Johannes; Jürimägi, Lembit; Raik, Jaan, Tallinn University of Technology, EE

11.30 **Lunch**

7.1 Amplifiers

Chair: Tor S. Lande, University of Oslo, NO

7.2 Low Power Systems

Chair: Jim Tørresen, University of Oslo, NO

12.30 Highly linear and reliable low band class-O RF power amplifier in 130 nm CMOS technology for 4G LTE applications
Khan, Muhammad Abdullah; Farouk Aref, Ahmed; Wei, Muh Dey; Negra, Renato, RWTH Aachen University, DE

A Comparison of Serial Interfaces on Energy Critical Systems
Solheim, Tharald; Grannæs, Marius, Silicon Labs, NO

12.50 A compact 0.3-10 GHz Broadband Stacked Amplifier in 65nm standard CMOS
Tarar, Mohsin Mumtaz; Wei, Muh-Dey; Negra, Renato, RWTH Aachen University, DE

Adaptive Power Monitoring For Self-aware Embedded Systems
El ahmad, Mohamad; Najem, Mohamad; Benoit, Pascal; Sassatelli, Gilles; Torres, Lionel, University of Montpellier, FR

13.10 An Ultra-Low-Voltage OTA in 28 nm UTBB FDSOI CMOS Using Forward Body Bias
Harikumar, Prakash; Wikner, J Jacob; Alvandpour, Atila, Linköping University, SE

Area and power savings via buffer reorganization in asymmetric 3D-NoCs for heterogeneous 3D-SoCs
Joseph, Jan Moritz; Blochwitz, Christopher; García-Ortiz, Alberto; Pionteck, Thilo, Universität zu Lübeck, DE

13.30 Low power, highly stable and wideband LNA for GNSS applications in SiGe technology
Deo, Navneeta; Wernehag, Johan; Thelberg, Joakim, Lund University, SE

Comparative Analysis of Flip-Flop Architectures for Subthreshold Applications in 28nm FDSOI
Låte, Even, Ali Asghar Vatanjou, Trond Ytterdal, Snorre Aunet NTNU, NO

13.50 Inductorless and cross-coupled wideband LNA with high linearity
Bierbüsse, David; Bousseaud, Pierre; Negra, Renato, RWTH Aachen University, DE

Microcontroller Energy Consumption Estimation Based on Software Analysis for Embedded Systems
Ruberg, Priit; Lass, Keijo; Ellervee, Peeter, Tallinn

University of Technology, EE

14.10 **Coffee**

14.40 **Invited talk: RIMFAX, a radar for the next NASA rover Mars 2020.**
Svein-Erik Hamran, Norwegian Defence Research Est./University of Oslo, NO

15.25 NORCAS 2016 announcement

15.30 Finish